CPU Core IPC Enhancements

- Advanced branch prediction
- 32B instruction fetch
- Sideband Stack Optimizer
- **Out-of-order load execution**
- TLB Optimizations
- Data-dependent divide latency
- More Fastpath instructions
  - CALL and RET-Imm instructions
  - Data movement between FP & INT
- Bit Manipulation extensions
  - LZCNT/POPCNT
- SSE extensions
  - EXTRQ/INSERTQ,
  - MOVNTSD/MOVNTSS

- **New technology allows load instructions to bypass:**
  - **Other loads**
  - **Other stores which are known not to alias with the load**
- **Significantly mitigates L2 cache latency**