CPU Core IPC Enhancements

- Advanced branch prediction
- 32B instruction fetch
- Sideband Stack Optimizer
- Out-of-order load execution
- **TLB Optimizations**
- Data-dependent divide latency
- More Fastpath instructions
  - CALL and RET-Imm instructions
  - Data movement between FP & INT
- Bit Manipulation extensions
  - LZCNT/POPCNT
- SSE extensions
  - EXTRQ/INSERTQ,
  - MOVNTSD/MOVNTSS

- **Support for 1G pages**
- **48bit physical address**
- **Larger TLBs key for:**
  - **Virtualized workloads**
  - **Large-footprint databases and transaction processing**
- **DTLB**
  - **Fully-associative 48-way TLB (4K, 2M, 1G)**
  - **Backed by L2 TLBs:**
    - ***512 x 4K, 128 x 2M***
- **ITLB**
  - **16 x 2M entries**