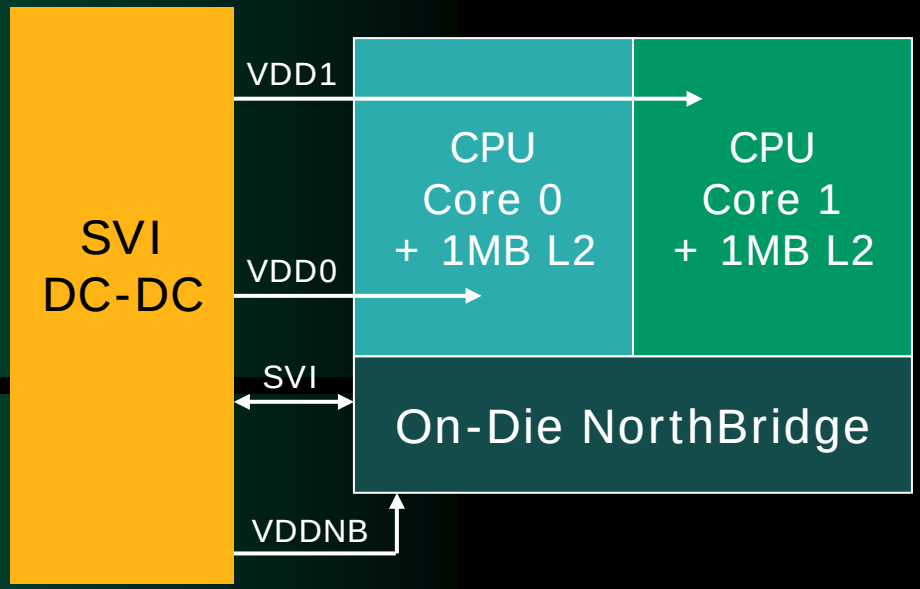
Voltage Planes and Control

Fixed Analog and I/O Voltage Planes

- VDDIO & VTT for DDR PHY
- VDDA for on-die PLL
- VLDT for HyperTransport PHY

Independently-Variable Voltage Planes

- VDD0 for CPU core 0
- VDD1 for CPU core 1
- VDDNB for on-die NorthBridge



Serial VID Interface (SVI) Protocol provides pin-efficient means to control multiple independent voltage planes